REMARKS/ARGUMENTS

Claims 1-21 remain in this application.

In Appl. No. 09/827,768, the Examiner rejected a claim that is equivalent to current claim 11. The claim was rejected as being anticipated by Aleksic et al. (U.S. Pat. No. 6,532,525; hereinafter "Aleksic"). Specifically, the Examiner asserted:

> As to claim 16 [now claim 11], Aleksic discloses the invention as claimed. Aleksic discloses a method of driving data from a memory controller (Fig. 1), comprising: a) providing data pad driver circuitry of said memory controller with a first data stream when said memory controller is configured to operate in a 1x mode (Fig. 1 DDR BUS); b) providing said data pad driver circuitry with N-1 additional data streams (Fig. 10 Ref. 240 and col. 10) when said memory controller is configured to operate in an Nx mode ($N \geq 2$) (Fig. 1 Ref. 14 and QDR BUS);. . .
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> Office Action in Appl. No. 09/827,768 dated 7/09/2003, p. 3.

Applicants note, however, that the DDR BUS and QDR BUS relied on by the Examiner in rejecting Applicants' claim are two different buses and, thus, the memory controller disclosed by Alexsic is not capable of generating either a 1x or Nx data stream at a single data pad, as set forth in Applicants' claim.

Applicants' claim 11 is believed to be allowable over Aleksic at least for the above reason. Applicants' claims 12-16 are believed to be allowable over Aleksic at least for the reason that they depend from an allowable claim 11.

In Appl. No. 09/827,768, the Examiner also rejected a claim that is equivalent to current claim 11. The claim was rejected as being anticipated by Mizuyabu et al. (U.S. Pat. No. 6,370,630; hereinafter "Mizuyabu"). Specifically, the Examiner asserted:

> As to claim 16 [now claim 11], Mizuyabu discloses a method of driving data from a memory controller (Fig. 1), comprising: a) providing data pad (col. 2 lines 55-60 and col. 2 line 36, port, pad and pin read on this limitation) driver circuitry of said memory controller with a first data stream when said memory controller is configured to operate in a 1x mode (Fig. 1 Ref. 122); b) providing said data pad driver circuitry with N-1

additional data streams when said memory controller is configured to operate in an Nx mode (N≥2) (Fig. 1 Ref. 150);. . .

Office Action in Appl. No. 09/827,768 dated 7/09/2003, p. 5.

Applicants note, however, that Mizuyabu's memory controller 114 communicates with processing unit 122 and memory 150 over two different buses and, thus, the memory controller disclosed by Mizuyabu is not capable of generating either a 1x or Nx data stream at a single data pad, as set forth in Applicants' claim.

Applicants' claim 11 is believed to be allowable over Mizuyabu at least for the above reason. Applicants' claims 12-16 are believed to be allowable over Mizuyabu at least for the reason that they depend from an allowable claim 11.

In Appl. No. 09/827,768, the Examiner further rejected a claim that is equivalent to current claim 1. The claim was rejected as being anticipated by Mizuyabu. However, Applicants believe claim 1 to be allowable over Mizuyabu for reasons that are similar to why claim 11 is believed to be allowable over Mizuyabu. Applicants' claims 2-9 are believed to be allowable over Mizuyabu at least for the reason that they depend from an allowable claim 1.

In Appl. No. 09/827,768, the Examiner also rejected a claim that is equivalent to current claim 17. The claim was rejected as being anticipated by Mizuyabu. However, Applicants believe claim 17 to be allowable over Mizuyabu for reasons that are similar to why claim 11 is believed to be allowable over Mizuyabu. Applicants' claims 18-21 are believed to be allowable over Mizuyabu at least for the reason that they depend from an allowable claim 17.

Respectfully submitted,
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